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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,449	01/21/2004	Tatsuya Kunikiyo	247943US2X	1383

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EXAMINER	
KRAMSKAYA, MARINA	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 11/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,449	KUNIKIYO ET AL.	
	Examiner	Art Unit	
	Marina Kramskaya	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *8-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I in the reply filed on 08/11/2005 is acknowledged. The traversal is on the ground(s) that invention Group I-IV are all classified in class 324. This is not found persuasive because despite the classification in the same class, the subject matter claimed diverges into several applications of capacitance measurement as set forth in the "subcombinations usable together" restriction requirement in the prior office action dated 07/13/2005.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al., US 6,404,222, in view of Chen, US 6,414,498.

As per Claim 1, Fan discloses a capacitance measurement circuit comprising:

a first terminal (the connection point of the first **m1** (520), between transistors 514 and 516), second (being at ground) and third terminals (the connection point of the second **m1** (518) between transistors 508 and 510), said first terminal being accompanied by a first capacitance (C_{wire} + C_x) including first capacitance component (C_x) to be measured (shown as 410 in block diagram of FIG. 4) and a non-target capacitance component (C_{wire}) not to be measured (shown as 412 in block diagram of FIG. 4), the third terminal being accompanied by a dummy capacitance (C_{wire}) having the same capacitance value as said non-target capacitance component (shown as "reference capacitor" 408 in block diagram of FIG. 4);

a first current detector (504) detecting a first current supplied to said first terminal;

a third current detector (502) detecting a third current supplied to said third terminal; and

a target capacitance forming section (**m1** + **m2**) formed between said first terminal and second terminal (ground terminal) so that said first terminal is accompanied by said first capacitance component (C_{wire} + C_x),

said target capacitance forming section (**m1 + m2**), said first (connection at **520**) to second terminals (ground terminal), and said first (**504**) to third (**502**) current detectors constituting a capacitance measurement section (see ABS., lines 1-6).

Fan does not disclose a second capacitance component to be measured (as part of the first capacitance), or a second current detector detecting a second current induced from said second terminal.

Chen discloses first (c_1) and a second capacitance component ($\mathbf{c_n}$) to be measured (as part of the first capacitance c_N, in the target capacitance forming section **104**). Chen also discloses a total current detector (**138**), which acts as a second current detector detecting a second current induced from said second terminal (**112** of 109-n).

Therefore, it would have been obvious to a person of ordinary skill in the art to include a second capacitance component for measurement and a second current detection unit, as taught by Chen, in the capacitance measuring system of Fan, in order to account for the capacitance produced by all the interconnections in an IC chip.

As per Claim 2, Fan discloses a capacitance measurement circuit as applied to claim 1, above, wherein

said first to third current detectors (**504** to **502**) include at least one transistor (transistors **506** and **512**),

said at least one transistor including a transistor which has a transistor characteristic of being less apt to cause a leakage current than an ordinary transistor which constitutes a logic circuit (i.e. the leakage current is reduced when the a gate-type

transistor is in the OFF stage, steps 1-6 on pages 6-7 provide for the sequential switching of the transistors, reducing the leakage current induced, and therefore reducing the error in capacitance measurement).

5. Claim 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. in view of Chen as applied to claim 1 above, and further in view of Oosawa wt al., US 6,597,191.

As per Claim 3, Fan discloses the capacitance measurement circuit as applied to claim 1, above, wherein

said first to third current detectors (**502** to **504**) include at least one transistor of a first conductivity type (transistors **506** and **512** both of P-type),

said at least one transistor being formed in a well region of a second conductivity type (a p-type transistor consists of a p-doped region in an n-type surface).

Fan does not explicitly disclose the structure of the testing circuit wherein the well region is selectively formed in an upper layer of a bottom region of the first conductivity type.

Oosawa discloses a testing circuit wherein the well region (n-well **72**) is selectively formed in an upper layer (20) of a bottom region of the first conductivity type (see FIG. 6).

Therefore, it would have been obvious to a person of ordinary skill in the art to form a transistor of a first conductivity type in a well region of a second conductivity type, as taught by Oosawa, in the testing circuit of Fan, for best element separation.

As per Claim 4, Fan discloses the capacitance measurement circuit as applied to claim 1, above, wherein

said first to third current detectors (**504** to **502**) include first and second transistors of different conductivity types (**512** PFET and **510** NFET).

Fan does not disclose

the first and second transistors being formed in a semiconductor layer of an SOI (Silicon-on-Insulator) substrate which is formed of a buried insulating layer and the semiconductor layer formed on the buried insulating layer,

the first and second transistors being isolated from each other by an element isolation region which extends to the buried insulating layer.

Oosawa discloses a test circuit structure wherein

the first and second transistors being formed in a semiconductor layer of an SOI (Silicon-on-Insulator, also referred to as "U-groove separation structure" in Oosawa reference: column 9, lines 13-14) substrate which is formed of a buried insulating layer (**75**) and the semiconductor layer (**72**) formed on said buried insulating layer,

the first and second transistors (see FIG. 6, numeral 71 designates a P-well region in which an N-channel MOSFET is formed; 72, an N-well region in which a P-

channel MOSFET is formed) being isolated from each other by an element isolation region (**54**) which extends to said buried insulating layer (**75**).

Therefore, it would have been obvious to a person of ordinary skill in the art to utilize a test circuit structure where the first and second transistors are formed on a layer of SOI substrate that is formed on a buried insulating layer, including an isolation layer between the transistors, as taught by Oosawa, in the circuit of Fan, in order to provide proper isolation between elements.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. in view of Chen as applied to claim 1 above, and further in view of Fried et al., US 6,624,651.

Fan discloses the capacitance measurement circuit as applied to claim 1, above, wherein

said capacitance measurement section includes a first circuit (FIG. 5),

said first circuit comprising said first (the connection point of the first **m1** (520), between transistors 514 and 516) to third (the connection point of the second **m1** (518) between transistors 508 and 510) terminals and said first to third current detectors (**504** and **502**),

said first circuit including, a target capacitance forming section (**m1** + **m2**),

said first capacitance component includes first and second partial capacitance components (C_{wire} + C_x),

said first target capacitance forming section (**m1** + **m2**) substantially includes said first and second partial capacitance components (C_{wire} + C_x).

Fan does not explicitly disclose a second circuit with a second target capacitance forming section, first and second target capacitance forming sections being different from each other, and second target capacitance forming section substantially including only said second partial capacitance component.

Fried et al., discloses multiple circuits (**130**, **135**, **140**, **145**, **150**, **155**) each testing a capacitance forming section, each target capacitance forming sections being different from each other, and second target capacitance forming section substantially including only said second partial capacitance component (FIG. 1, column 4, lines 32-36).

Therefore, it would have been obvious to a person of ordinary skill in the art to duplicate the capacitance measurement circuit, as taught by Fried, in the circuit of Fan, wherein in the target capacitance forming section would be representative of additional interconnections in an IC chip for the purpose of measuring additional target capacitance segments.

Allowable Subject Matter

7. Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As per Claim 6, the prior art fails to anticipate or make obvious in combination a capacitance measuring circuit particularly characterized in

a first measurement transistor, wherein a distance from the gate electrode to a contact hole is set to a length with which the first partial capacitance component is effective, and

a second measurement transistor, wherein a distance from said gate electrode to said contact hole is set to a length with which the first partial capacitance component is ineffective.

As per Claim 7, the prior art fails to anticipate or make obvious in combination a capacitance measuring circuit particularly characterized in

a first measurement transistor, wherein the first and second contact holes are formed such that the first partial capacitance component is effective, and

a second measurement transistor, wherein at least one of the first and second contact holes is formed such that said first partial capacitance component is zero.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Froment, US 6,366,098, discloses a test structure for measuring capacitance values through current detection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571)272-2180. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Marina Kramskaya
Examiner
Art Unit 2858

MK

ANJAN DEB
PRIMARY EXAMINER